IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
	)	
Chih-Ming Tsai	)	Group Art Unit: 2116
	)	
Serial No.: 10/780,934	)	Examiner: Stoynov, Stefan
	)	
Filed: February 17, 2004	)	Confirmation No.: 1904
	)	
For: System and Method for Actively Booting a Computer System	)	TKHR Docket: 250915-1010
	)	Top-Team: 0719-9462US
	)	

AMENDMENT AND RESPONSE TO OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The Office Action mailed May 15, 2006 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A system for actively booting a computer system, electrically connected with a storage medium which stores boot codes thereon for initiating an operating system of the computer system, and said system comprising:

a non-XIP type storage medium controller accessing the boot codes from the storage medium when said storage medium is a non-XIP type storage medium;

an internal buffer coupled to the non-XIP type storage medium controller, storing the boot codes accessed from the non-XIP type storage medium; and

a multiplexing storage medium controller coupled to the internal buffer, controlling a central processing unit (CPU) disposed in the computer system to access the boot codes from the internal buffer to initiate the operating system of the computer system.

2. (Original) The system as claimed in claim 1 wherein the multiplexing storage medium controller disables the CPU before the non-XIP type storage medium controller accesses the boot codes.

3. (Original) The system as claimed in claim 2 wherein the multiplexing storage medium controller re-activates the CPU when the non-XIP type storage medium controller accesses and stores the boot codes successfully from the non-XIP type storage medium.

4. (Original) The system as claimed in claim 1 wherein the multiplexing storage medium controller accesses the boot codes directly from the storage medium to the CPU for initiating the operating system when said storage medium is an XIP type storage medium.

5. (Original) The system as claimed in claim 1 wherein the non-XIP type storage medium is a NAND-type flash memory.

6. (Original) A method for actively booting a computer system, with access of boot codes from a storage medium to initiate an operating system of a computer system, comprising steps of:

determining whether the storage medium is a XIP type storage medium;

a CPU disposed in the computer system directly accessing the boot codes directly from the storage medium through a multiplexing storage medium controller when said storage medium is the XIP type storage medium;

facilitating a non-XIP type storage medium controller to access the boot codes from the storage medium and then to store the boot codes in an internal buffer, and controlling the CPU to access the boot codes from the internal buffer when said storage medium is a non-XIP type storage medium; and

the CPU implementing the boot codes to initiate the operating system of the computer system.

7. (Original) The method as claimed in claim 6 wherein the step of controlling the CPU further comprising: disabling the CPU by the multiplexing storage medium controller before the non-XIP type storage medium controller accesses the boot codes from the storage medium when said storage medium is a non-XIP type storage medium.

8. (Original) The method as claimed in claim 7 wherein the step of controlling the CPU further comprising: re-activating the CPU when the non-XIP type storage medium controller accesses and stores the boot codes successfully from the storage medium.

9. (Original) The method as claimed in claim 6 wherein the non-XIP type storage medium is a NAND-type flash memory.

10. (Original) A computer system providing a method for actively enabling the computer system, and said method comprising the steps of:

determining whether the storage medium is a XIP type storage medium;

a CPU disposed in the computer system accessing the codes directly from the storage medium through a multiplexing storage medium controller when said storage medium is a XIP type storage medium;

facilitating a non-XIP type storage medium controller to access the codes from the storage medium and then to store the codes in an internal buffer, and controlling

the CPU to access the codes from the internal buffer when said storage medium is a non-XIP type storage medium; and

the CPU implementing the accessed codes in the computer system.

11. (Original) The method as claimed in claim 10 wherein the multiplexing storage medium controller disables the CPU before the non-XIP type storage medium controller accesses the codes from the storage medium when said storage medium is a non-XIP type storage medium.

12. (Original) The method as claimed in claim 10 wherein the multiplexing storage medium controller re-activates the CPU when the non-XIP type storage medium controller accesses and stores the codes successfully from the storage medium.

13. (Original) The method as claimed in claim 10 wherein the non-XIP type storage medium is a NAND-type flash memory.

REMARKS

The Examiner is thanked for the thorough examination of this application, and the indication that claims 2, 3, 7, 8, 11, and 12 contain allowable subject matter. Claims 1-13 remain pending in the application.

Claims 1, 4, and 5 stand rejected under 35 U.S.C. 102(e) as allegedly anticipated by Tang et al., US Patent Appl. Pub. No. 2003/0206442. Claims 6, 9, 10, and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Tang in view of Hatalkar, US Patent Appl. Pub. No. 2004/0088701. For at least the reasons that follow, Applicant respectfully request reconsideration and withdrawal of the rejections.

Fundamental Distinction between Cited References and Claimed Embodiments

Applicant respectfully traverses the rejections of claims 1-13 of the present application for reasons that will be specifically addressed in following paragraphs. However, before addressing the details of specific rejections, Applicant notes that there are fundamental differences between the citations of Tang and Hatalkar and that of the claimed embodiments.

The presently claimed embodiments are generally directed to methods for actively booting a computer system with access of boot codes from a storage medium to initiate an operating system of a computer system. The embodiments comprise **determining whether the storage medium is a XIP type storage medium**; a CPU disposed in the computer system **directly accessing the boot codes directly from the storage medium** through a multiplexing storage medium controller **when said storage medium is the XIP type storage medium**; **facilitating a non-XIP type storage medium controller to access the boot codes from the storage medium and then to store the boot codes in an internal buffer**, and controlling the

CPU to **access the boot codes from the internal buffer when said storage medium is a non-XIP type storage medium**; and the CPU implementing the boot codes to initiate the operating system of the computer system.

In contrast, Tang discloses a flash memory bridging device connected to a NOR flash memory interface for using a NAND flash memory to simulate the operation of a NOR flash memory, comprising: a buffer region for storing data corresponding to a portion of the address of the NAND flash memory, and a control logic unit coupled to the buffer region for receiving a memory instruction, executing the instruction and responding to the request of the memory instruction. Hatalkar discloses a method for dynamic management of execute in place applications, comprising gathering application usage data, and configuring at least one or more applications as execute-in-place or non-execute-in-place based upon the application usage data.

The claimed embodiments, however, focus on selectively accessing boot codes from either an XIP type or non-XIP type memory devices attached in the computer system to initiate an operating system of the computer system. Neither of the cited references discloses this feature. For at least this reason, the rejections should be withdrawn.

Discussion of Rejection of Claim 1

The Office Action rejected claim 1 as allegedly anticipated by Tang. As supported by at least Fig. 1 of the present application, claim 1 recites:

> 1. (Original) A system for actively booting a computer system, electrically connected with a storage medium which stores boot codes thereon for initiating an operating system of the computer system, and said system comprising:
>
> ***a non-XIP type storage medium controller accessing the boot codes from the storage medium when said storage medium is a non-XIP type storage medium;***

> ***an internal buffer coupled to the non-XIP type storage medium controller, storing the boot codes accessed from the non-XIP type storage medium;*** and
> a multiplexing storage medium controller coupled to the internal buffer, controlling a central processing unit (CPU) disposed in the computer system ***to access the boot codes from the internal buffer to initiate the operating system of the computer system.***

As emphasized above, the multiplexing storage medium controller of the claimed embodiment enables the CPU to access the boot codes from the internal buffer via the non-XIP type storage medium controller to initiate the operating system of the computer system when a storage medium storing the boot codes is the non-XIP type storage medium or directly access the boot codes when a storage medium storing the boot codes is the XIP type storage medium. In contrast, Tang only teaches a NAND flash memory.

The Office Action cited paragraphs 0022 and 0024 of Tang as teaching the features emphasized above. These paragraphs actually state:

> [0022] FIG. 2 is a schematic diagram showing the application of a flash memory bridging device according to one preferred embodiment of this invention. As shown in FIG. 2, the system includes a memory control chip 210, a NAND flash memory 230 for storing program codes and a flash memory bridging device 220. The flash memory bridging device 220 is coupled to the memory control chip 210 and the NAND flash memory 230. The flash memory bridging device uses the NAND flash memory 230 to simulate the operation of a NOR flash memory so that the performance and reliability demanded for storing program code is attained. Obviously, anyone familiar with memory partitioning may divide the NAND flash memory 230 into separate regions for holding program codes and data.
>
> [0024] The control logic unit 320 further includes a buffer access unit 325, a buffer control logic unit 330, a second buffer access unit 335, an error correction code unit 340, a block address translation table unit 345, a NAND flash memory control unit 350 and a main control logic unit 355. The first buffer access unit 325 serves a similar function to the NOR flash memory interface within the memory control chip 210 as shown in FIG. 2 as an access interface with the buffer region 310. The buffer control logic unit 330 is coupled to the first buffer access unit 325, the second buffer access unit 335 and the buffer region 310 for controlling reading/writing in the buffer region 310. The second buffer access unit 335 is

coupled to the buffer control logic unit 330 to serve a similar function to the NAND flash memory 230 as shown in FIG. 2 as an access interface for the buffer region 310. The error correction code unit 340 is coupled to the second buffer access unit 335 for correcting read-out data from the NAND flash memory as shown in FIG. 2. The block address translation table unit 345 is coupled to the second buffer access unit 335 for converting a logic address from the memory instruction into an actual address. The NAND flash memory control unit 350 is coupled to the error correction code unit 340 and the block address translation table unit 345 for actually reading/writing data to/from the NAND flash memory 230. The main control logic unit 355 is coupled to the first buffer access unit 325, the second buffer access unit 335 and the block address translation table unit 345. The main control logic unit 355 controls the reading of data not yet registered inside the buffer region 310 from the NAND flash memory 230, determines if the requested data of a memory instruction is already in the buffer region 310 or not and controls the steps for writing stored data from the buffer region 310 to the NAND flash memory 230.

As can be readily verified from even a cursory review of the above-quoted sections of Tang, there is no teaching whatsoever of selectively accessing boot codes from either an XIP type or non-XIP type memory devices. For at least the foregoing reasons, the rejection of claim 1 should be withdrawn. Insofar as claims 4 and 5 depend from claim 1, the rejections of these claims should be withdrawn for at least the same reason.

Rejection of Independent Claims 6 and 10

Independent claims 6 and 10 recite:

> 6. A method for actively booting a computer system, with access of boot codes from a storage medium to initiate an operating system of a computer system, comprising steps of:
>
> ***determining whether the storage medium is a XIP type storage medium;***
>
> ***a CPU disposed in the computer system directly accessing the boot codes directly from the storage medium through a multiplexing storage medium controller when said storage medium is the XIP type storage medium;***
>
> ***facilitating a non-XIP type storage medium controller to access the boot codes from the storage medium and then to store the boot codes in an internal buffer, and controlling the CPU to access the boot codes from the internal buffer when said storage medium is a non-XIP type storage medium;*** and

the CPU implementing the boot codes to initiate the operating system of the computer system.

10. A computer system providing a method for actively enabling the computer system, and said method comprising the steps of:

determining whether the storage medium is a XIP type storage medium;

a CPU disposed in the computer system accessing the codes directly from the storage medium through a multiplexing storage medium controller when said storage medium is a XIP type storage medium;

facilitating a non-XIP type storage medium controller to access the codes from the storage medium and then to store the codes in an internal buffer, and controlling the CPU to access the codes from the internal buffer when said storage medium is a non-XIP type storage medium; and

the CPU implementing the accessed codes in the computer system.

Like in the rejection of claim 1, the Office Action cited paragraph 0024 of Tang as allegedly teaching the features emphasized above. Paragraph 0024 has been quoted above, and as can be readily verified, there is no teaching in paragraph 0024 of determining whether the storage medium is a XIP type storage medium, or accessing codes directly from the storage medium through a multiplexing storage medium. For at least the foregoing reasons, the rejection of claim 6 should be withdrawn. Insofar as claim 9 depends from claim 6 and claim 13 depends from claim 10, these claims should be allowed as well.

As a separate and independent basis for the patentability of claims 6, 9, 10, and 13, Applicant respectfully traverses the rejections as failing to identify a proper basis for combining the cited references. In combining these references, the Office Action stated only that the combination would have been obvious "in order to increase the memory speed or decrease the required memory space when using XIP and non-XIP types of memories." (Office Action, page 6). This alleged motivation is clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a system for actively booting a computer, as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

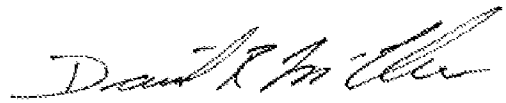
CONCLUSION

For at least the reasons described above, all claims are in condition for allowance.

Should Examiner feel that a telephone discussion would expedite the examination of this application, the Examiner is invited to contact the undersigned attorney.

No fee is believed to be due in connection with this Amendment and Response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

Daniel R. McClure, Reg. No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500